REMARKS

Favorable reconsideration of this application in light of the following discussion is respectfully requested.

Claims 1-30 are presently active in this case. The present Amendment amends Claims 1-6 and 16-21 without introducing any new matter.

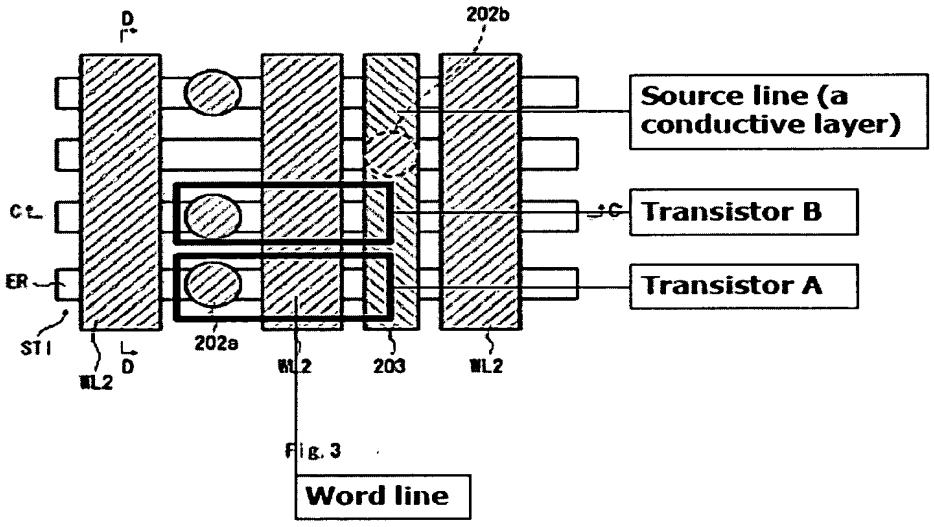
The outstanding Office Action objected to the Abstract of the Disclosure and Claims 1-30 because of informalities. Claims 1, 2, 6, 16-17 and 19-21 were rejected under 35 U.S.C. §102(e) as anticipated by Hirai et al. (U.S. Patent No. 6,703,676, herein "Hirai"). Claims 3-5 were rejected under 35 U.S.C. §103(a) as unpatentable over Hirai in view of Harada et al. (U.S. Publication No. 2001/0008311, herein "Harada"). Claims 7-15 and 22-30 were rejected under 35 U.S.C. §103(a) as unpatentable over Hirai in view of Noda et al. (U.S. Patent No. 6,731,538, herein "Noda").

In response to the objections to the Abstract and Claims 1-30, the Abstract of the Disclosure and Claims 1-6 and 16-21 are amended to correct the noted informalities. In light of their formal nature, the changes to the Abstract do not raise a question of new matter.

To clarify Applicants' invention, independent Claim 1 is amended to recite "an element isolation region formed in an upper portion of the semiconductor substrate and arranged between the first and second memory cells" and to recite "the conductive layer formed to be contact with the element isolation region that is arranged between the second diffusion layer of the first memory cell and the fourth diffusion layer of the second memory cell." Further, independent Claim 16 is amended to recite "wherein the height of the conductive layer is approximately uniform." These features find non-limiting support in the disclosure as originally filed, for example from page 8, line 11 to page 9, line 4 and in Figures 1 and 3-4.

In response to the rejections of Claims 1-30 under 35 U.S.C. §102(e) and 35 U.S.C. §103(a), Applicants respectfully request reconsideration of these rejections and traverse the rejections, as discussed next.

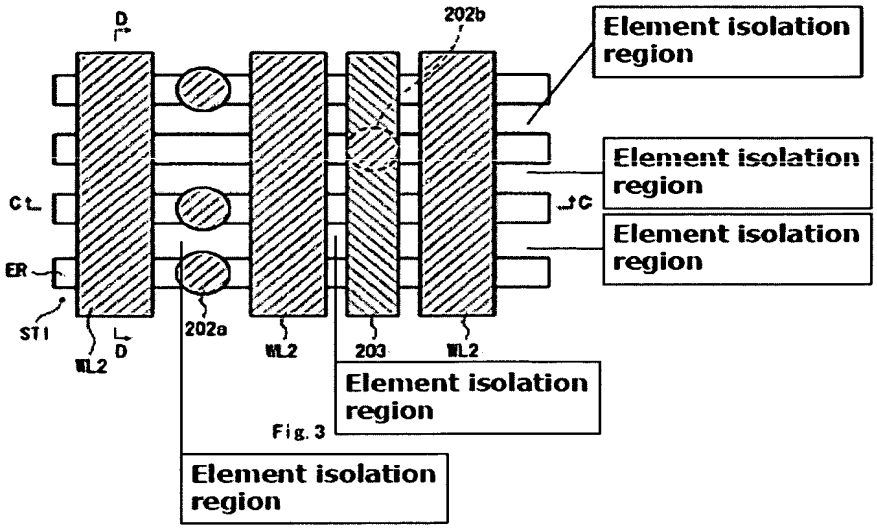
To facilitate the understanding of the Applicants' invention, the present invention as disclosed in the Specification and in the Figures is next explained. Applicants' Figure 3 shows a top view of the non-volatile memory device. This Figure is shown below, marked-up with two black solid squares showing transistors A and B, so as to better explain how Applicants' invention is believed to be patentably distinct over the references of record. Each transistor has diffusion layers serving as source and drain electrodes.[1]



Applicants' Figure 3 showing transistors A and B, word line and source line

Further, element isolation regions are formed between the transistors. As shown in the next Figure below, there is an element isolation region formed between transistors A and B. A source line 203 is arranged for both transistors A and B, also formed to be in contact with the element isolation region that is arranged between the transistors A and B.[2]

[1] See Applicants' Figure 4.
[2] See Applicants' Specification, at page 6, lines 17-21 and in the Figures 2 and 3.



Applicants' Figure 3 showing the element isolation regions

Turning now to the primary reference used in the outstanding Office Action to form all the rejections, Hirai discloses a magnetic memory device with gate electrodes 4 formed above the semiconductor substrate 1 with gate insulation films 3 formed between them.[3] However, Applicants respectfully submit that Hirai fails to teach or suggest the second gate electrode of the second memory cell being electrically connected to the first gate electrode of the first memory cell, as claimed in independent Claim 1. In other words, Hirai fails to disclose that one word line WL2 is arranged for both transistors A and B. As shown in Hirai, an interlayer insulating film 7 made of SiO_2 is formed on the substrate where the transistor structures are formed.[4] Therefore, an interlayer isolation film and a gate isolation film configured to isolate the gates of a transistor, as taught by Hirai, ***is not*** a second gate electrode of the second memory cell electrically connected to the first gate electrode of the first memory cell, as claimed.

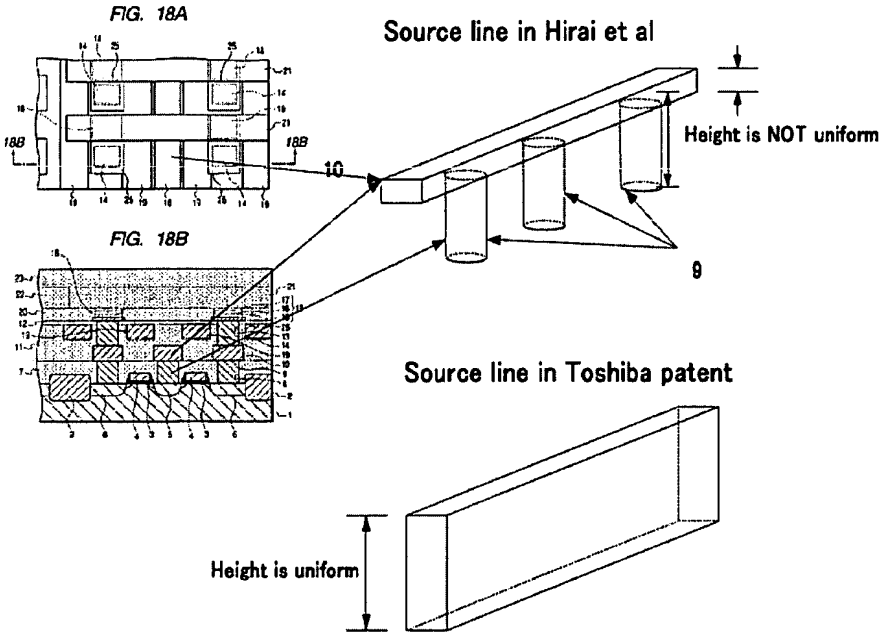
Applicants also submit that Hirai fails to teach or suggest that the conductive layer is formed to be contact with the element isolation region arranged between the second diffusion

[3] See Hirai in the Abstract, at column 5, lines 48-57 and in Figures 1A, 1B, 18A and 18B.
[4] See Hirai at column 7, lines 54-57 and in corresponding Figure 2A.

layer of the first memory cell and the fourth diffusion layer of the second memory cell, as recited in amended Claim 1. In other words, a source line 203 is arranged for both the transistors A and B and is also formed to be in contact with the element isolation region arranged between the diffusion layers of transistors A and B.[5] Therefore, the height of source line 203 is approximately uniform, as shown in the next Figure. Amended independent Claim 16 also recites that the height of the conductive layer is approximately uniform.

Hirai shows in Figures 18A and 18B two transistors, each of which have a gate electrode 4, a gate insulation film 3, a source region 5 and a drain region, arranged on a semiconductor substrate 1. Further, Figure 18B shows three plugs 9 which are formed by filling the contact holes 8.[6] The intermediate plug of the three plugs 9 is arranged between two gate electrodes 4. As further shown in Hirai's Figures 4A and 4B, element isolation regions 2 are arranged to isolate a pair of transistors including the elements 3, 4, 5 and 6, and the element isolation regions are arranged between the diffusion layers 5 and 6. Hirai's three holes 8 or plugs 9 are leading to the diffusion layers 5 and 6, therefore they ***are not*** leading to the element isolation regions.[7] Accordingly, Hirai's source line includes not only the first metal wiring 10, but also the plugs 9. Therefore, Hirai's source line does not have a uniform height, as illustrated in the Figure below.

[5] See Applicants' Figure 3.
[6] See Hirai at column 7, lines 62-67 and in Figures 3B, 4B and 18B.
[7] See Hirai in the Figures 3B, 4B, ... , 12B.



Uniform height of Applicants' source line

The references Harada and Noda, used by the outstanding Office Action as secondary references to form the 35 U.S.C. §103(a) rejections, do not remedy the deficiencies of Hirai, as next discussed.

Harada teaches that contact holes 8 are formed at predetermined positions into the underlying insulation layer so as to provide ohmic contact with the diffusion region 5.[8] The contact holes 8 are subsequently filled with tungsten and then a metal wiring 9 is formed onto the filled contact holes.[9] Therefore, Harada ***fails to teach or suggest*** that that the conductive layer is formed to be contact with the element isolation region that is arranged between the second diffusion layer of the first memory cell and the fourth diffusion layer of the second memory cell.

Noda's invention is concerned about page latch for nonvolatile semiconductor memory devices, and is entirely silent on structural features of the semiconductor memory.

[8] See Harada at page 5, paragraph 90.
[9] See Harada at page 5, paragraph 91-94 and in corresponding Figure 2B.

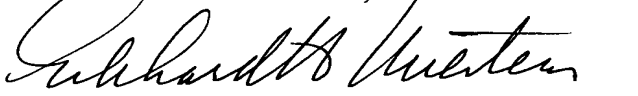
Therefore, even if the combination of Hirai and Harada and/or Noda is assumed to be proper, the combination fails to teach every element of the claimed invention. Specifically, the combination fails to teach the claimed second gate electrode of the second memory cell electrically being connected to the first gate electrode of the first memory cell, and also fails to teach or suggest the conductive layer being formed to be contact with the element isolation region that is arranged between the second diffusion layer of the first memory cell and the fourth diffusion layer of the second memory cell. Accordingly, Applicants respectfully traverse, and request reconsideration of, this rejection based on these patents.[10]

Consequently, in view of the present Amendment, no further issues are believed to be outstanding in the present application, and the present application is believed to be in condition for formal Allowance. A Notice of Allowance for Claims 1-30 is earnestly solicited.

Should the Examiner deem that any further action is necessary to place this application in even better form for allowance, the Examiner is encouraged to contact Applicants' undersigned representative at the below listed telephone number.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Eckhard H. Kuesters
Attorney of Record
Registration No. 28,870

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 06/04)

I:\ATTY\NS\00039\239515US\239515US-AM3-DRAFT1.DOC

[10] See MPEP 2142 stating, as one of the three "basic criteria [that] must be met" in order to establish a *prima facie* case of obviousness, that "the prior art reference (or references when combined) must teach or suggest all the claim limitations," (emphasis added). See also MPEP 2143.03: "All words in a claim must be considered in judging the patentability of that claim against the prior art."